IN THE CLAIMS:

Please amend claims 1, 7, 12 and 14 to read as follows:

1. (Twice Amended) A semiconductor memory device, comprising:

a semiconductor substrate, a gate electrode formed on the semiconductor substrate, and a plurality of source/drain junctions formed in the semiconductor substrate;

an interlayer insulating layer formed over the semiconductor substrate;

C1 a plug formed in the interlayer insulating layer, the plug including a diffusion barrier layer and a seed layer for electro plating;

a lower electrode of a capacitor contacted to the seed layer, wherein the lower electrode is formed by using an electro plating technique while imposing a current density of 0.1 - 20 mA/cm^2 with DC or a DC pulse to the semiconductor memory device;

a dielectric layer formed on the lower electrode; and

an upper electrode formed on the dielectric layer.

7. (Twice Amended) A method for fabricating semiconductor memory device, comprising the steps of:

C2 providing a semiconductor substrate, forming a gate electrode on the semiconductor substrate, and forming a plurality of source/drain junctions in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer and forming contact hole;

forming a plug in the contact hole, wherein the plug includes a diffusion barrier layer and a seed layer for electro plating;

forming a lower electrode of a capacitor contacted to the seed layer by using an electro plating technique while imposing a current density of 0.1 - 20 mA/cm^2 with DC or a DC pulse to the semiconductor memory device;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.

12. (Twice Amended) A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, forming a gate electrode on the semiconductor substrate, and forming a plurality of source/drain junctions in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer and forming a contact hole;

forming a plug in the contact hole, wherein the plug includes a diffusion barrier layer and a seed layer for electro plating;

forming a glue layer on the seed layer and the interlayer insulating layer;

forming a sacrificial layer on glue layer;

etching the sacrificial layer and the glue layer and forming an opening defining a region of a lower electrode of a capacitor;

C3 cont'd

forming the lower electrode on the seed layer in the opening, by using an electro plating technique while imposing a current density of 0.1 - 20 mA/cm^2 with DC or a DC pulse to the semiconductor memory device;

removing the sacrificial layer and the glue layer;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.

14. (Amended) The method as recited in claim 13, the step of providing the semiconductor substrate including:

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forming a conducting layer on the semiconductor substrate, wherein the conducting layer is used as an electrode in the step of forming the lower electrode.